HIGH VOLTAGE DRIVERS WITH FAST AMPLITUDE MODULATION – DP-FAM

Features

- HV pulse repetition rate up to 500 kHz
- Fast amplitude modulation of HV pulses
- Output HV pulse amplitude ranges from 0.1 kV to 2.5 kV

DP-FAM series drivers allow to control the amplitude of each HV output pulse with specific user-defined amplitude levels. The control is realized by one or two trigger-sync pulses and analog signal for amplitude modulation (HV program).


DP-FAM Pockels cell driver

Configuration samples of DP-FAM series encased drivers

CATALOGUE NUMBER OF DRIVER		DP-FAM-250-2.5-Al	DP-FAM-500-2.5-Al
HV operation voltage range		0.1 - 2.5 kV	
HV program input signal range		0.1 - 4.9 V	
Maximal HV repetition rate		250 kHz	500 kHz
HV pulse duration		70 – 3000 ns	70 – 1000 ns
HV pulse rise time, typical [1]		< 26 ns	
HV fall time, typical [1]		< 13 ns	
Output polarity		positive	
External trigger pulse requirements	Amplitude on 50 Ω	3.5 – 5 V	
	Rise/fall time	< 10 ns	
HV power consumption		60 W	120 W
24 VDC power consumption		<12 W	
Recommended HV power supply model		PS-80-2.6 (OEM type) HVS100-80-2.6 (lab type)	PS-120-2.6 (OEM type) HVS100-120-2.6 (lab type)
Dimensions		139 × 69 × 57 mm (Fig. 19)	
Cooling [2]		conductive or water	
Control interface [3]		CAN	

[1] All specifications are given for 6 pF Pockels cell load.

[2] Heat sink temperature must not exceed 35 °C (95 °F) in all regimes of operation.

[2] Requires USB-CAN converter for computer control that is sold separately.
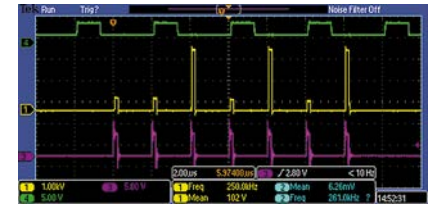
Example of driver operation.
Green trace – modulated analog input signal, purple trace – trigger signal SYNC (single pulse control mode), yellow trace – HV pulse.
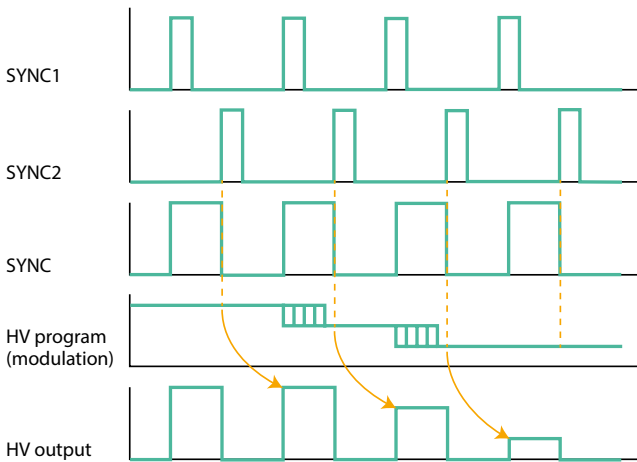
Operation timing charts.
SYNC1 and SYNC2 are used for 2-pulses control operation mode. HV program input amplitude is readout at SYNC2 rising edge and is used to set HV output amplitude for next HV output pulse which is started with SYNC1 rising edge. SYNC is used for single pulse control mode. HV program input amplitude is readout at SYNC falling edge and is used to set HV output amplitude for next HV output pulse which is started with SYNC rising edge.
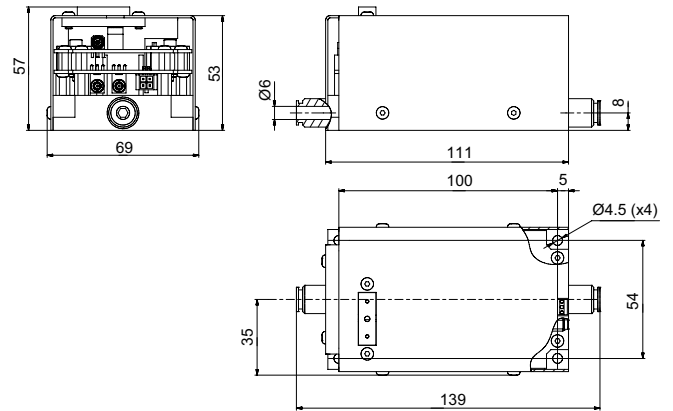

Fig. 19. Outline drawing of DP-FAM series drivers.